Table A3-5 Memory attribute summary (continued)

Memory type	Implementation includes LPAE[a]?	Shareability	Cacheability
Device	Yes	Outer Shareable	-
	No	Outer Shareable	
		Inner Shareable	
		Non-shareable	
Normal	-	Outer Shareable	One of: • Non-cacheable • Write-Through Cacheable • Write-Back Cacheable.
		Inner Shareable	
		Non-shareable	

a. LPAE means the Large Physical Address Extension.

Memory model and memory ordering on page AppxO-2593 compares these attributes with the memory attributes in architecture versions before ARMv6.

A3.5.3 Atomicity in the ARM architecture

Atomicity is a feature of memory accesses, described as *atomic* accesses. The ARM architecture description refers to two types of atomicity, defined in:

- *Single-copy atomicity*
- *Multi-copy atomicity* on page A3-129.

Single-copy atomicity

A read or write operation is *single-copy atomic* if the following conditions are both true:

- After any number of write operations to a memory location, the value of the memory location is the value written by one of the write operations. It is impossible for part of the value of the memory location to come from one write operation and another part of the value to come from a different write operation.
- When a read operation and a write operation are made to the same memory location, the value obtained by the read operation is one of:
  - the value of the memory location before the write operation
  - the value of the memory location after the write operation.

  It is never the case that the value of the read operation is partly the value of the memory location before the write operation and partly the value of the memory location after the write operation.

In ARMv7, the single-copy atomic processor accesses are:

- all byte accesses
- all halfword accesses to halfword-aligned locations
- all word accesses to word-aligned locations
- memory accesses caused by `LDREXD` and `STREXD` instructions to doubleword-aligned locations.

`LDM`, `LDC`, `LDC2`, `LDRD`, `STM`, `STC`, `STC2`, `STRD`, `PUSH`, `POP`, `RFE`, `SRS`, `VLDM`, `VLDR`, `VSTM`, and `VSTR` instructions are executed as a sequence of word-aligned word accesses. Each 32-bit word access is guaranteed to be single-copy atomic. The architecture does not require subsequences of two or more word accesses from the sequence to be single-copy atomic.